sames

PRELIMINARY

SA7110

READ-ONLY RF TRANSPONDER

FEATURES

- EEPROM flexibility of data and mode configuration
- 64 bits of OTP data factory programmed and locked
- Customer specific configuration of stored data
- Manchester or PSK mode custom set at factory
- Minimum external component count
- On-chip rectifier for powering up from RF signal
- On-chip data modulator
- On-chip high voltage protection / regulation
- On-chip RF frequency extractor / prescaler
- External tank resonance capacitor for RF resonance
- Sufficient distance without resonance capacitor
- Outputs data automatically after power-up
- Low power dissipation
- Small size
- No external storage capacitor required

DESCRIPTION

This device is manufactured in the SAMES 1.2µm N-well EEPROM process. It has 64bits of factory pre-programmed and locked bits in EEPROM memory. Its mode of operation is factory pre-programmed and locked in additional EEPROM. The mode of operation is either manchester coded or Phase Shift Keyed (PSK) coded.

The device has an on-chip rectification circuit that converts the incoming rf signal to DC power feeding V_{DD}. There is also an on-chip data modulator which works in conjunction with the rectifier. The time base is extracted by an on-chip RF clock extractor. High voltage protection is provided internally to protect against high voltages from the coil. The energy is stored on capacitance on chip due to low internal power consumption. These features result in a low external component count.

Data is read at the RF interface by means of the on-chip modulator. The stored bits are clocked out sequentially during the read operation. An internal power-on reset is provided which allows the device to start reading out data at low voltages for improved tag range.

PAD CONNECTIONS

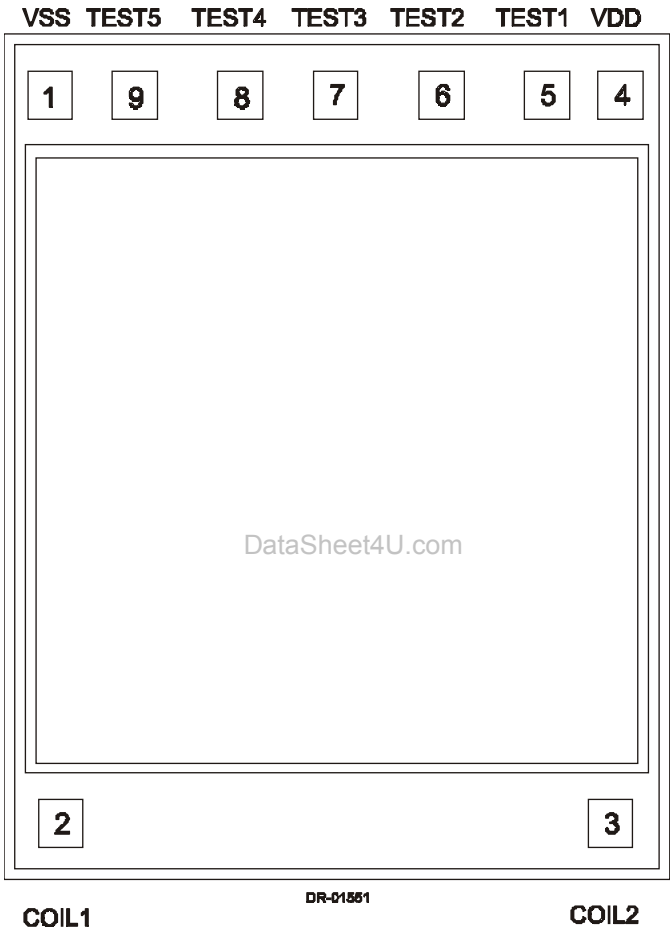


Figure 1

BLOCK DIAGRAM

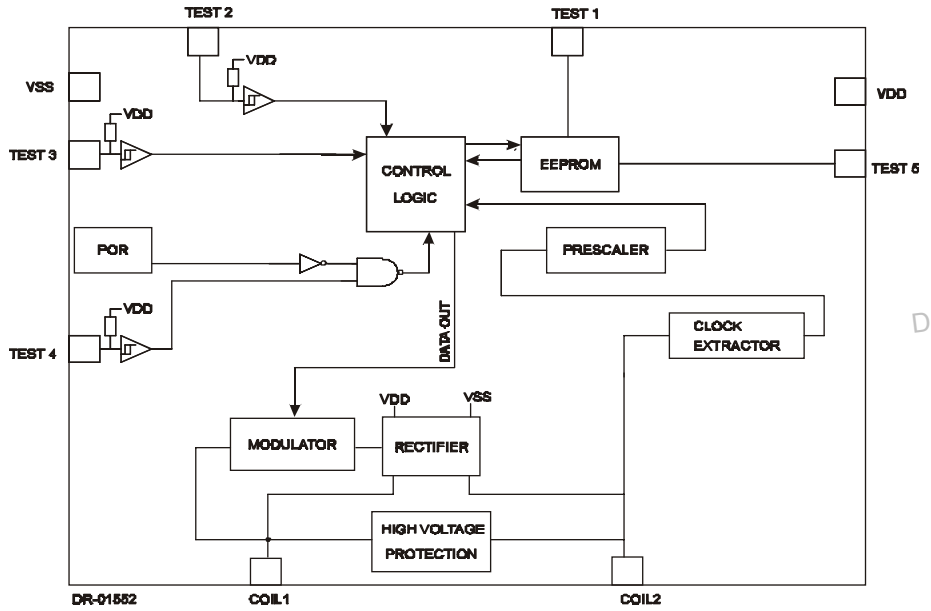


Figure2

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD}	-0.3	9.4	V	1, 2, 3, 4, 5
ESD protection	V_{pesd}	-	TBD	V	3, 8
Peak voltage across COIL1 or COIL2 to V_{SS}	$V_{COIL1,2}$ - V_{SS}	-10	+10	V	3, 6
Peak current through COIL 1,2	$I_{COIL1,2}$	-30	+30	mA	3, 7
Storage temperature	Tst	-55	+125	°C	3
Operating temperature	Top	-40	+70	°C	3

Note 1: Duration not to exceed 10 seconds, and no logic switching.

Note 2: Referenced to Vss

Note 3: Stresses above those listed under " absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating conditions section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Note 4: V_{DD} level when absolute maximum current goes through coil inputs.

Note 5: V_{DD} level when absolute maximum voltage is across coil inputs.

Note 6: Maximum peak voltage at COIL1 or COIL2 of incoming RF signal with V_{SS} as reference. Clamping by front end protection circuitry.

Note 7: Maximum allowed peak current of incoming RF signal.

Note 8: TBD - To be determined.

ELECTRICAL CHARACTERISTICS

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Chip dynamic current	I_{DD}		3	6	µA	V_{DD} = 3V
Static current for total chip	I_{DDS}		<1	TBD	µA	V_{DD} = 3V Clock stopped, COIL1, and COIL2 shorted to V_{SS}
Electrostatic Protection	V_{ESD}	-		TBD	V	C = 100pF R = 1.5Kohm
Voltage when POR comes out of rest	V_{POR}	<2	-	<3	V	During power-up V_{DD} - V_{SS} rising
Histereses on POR	V_{PORH}	200	-	600	mV	Between coming out of reset and going back into reset
Data Retention	T_{DR}	10	-	-	years	programmed
Supply Voltage	V_{DD}	2	-	8 Note1	V	At specified current at COIL1 and COIL2

Note 1: Maximum voltage is defined when forcing 10 mA on the coil inputs.

AC Operating Conditions

Clocking

Parameter	Symbol	Min	Typ	Max	Unit	Condition
RF carrier frequency required at COIL1, 2	f_{RF} = $1/T_{RF}$	50	125	400	KHz	Sustained RF in read mode
Number of RF carrier clock periods per data bit						
Manchester	N_M	-	64	-		
PSK	N_P	-	16	-		

Coil Inputs

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Unmodulated Low Level Input Voltage at COIL1, COIL2	V_{ILU}	-0.7	-0.65	-0.6	V	Peak level referenced to V_{SS}
Unmodulated High Level Input Volrage at COIL1, COIL2	V_{IHU}			8	V	Peak level referenced to V_{SS} I_{COIL} = 5mA
Modulated Low Level Input Volrage at COIL1, COIL2	V_{ILMI}	-0.7	-0.65	-0.6	V	Peak level referenced to V_{SS}
Modulated High Level Input Volrage at COIL1, COIL2	V_{IHMI}			2.4	V	Peak level referenced to V_{SS} I_{COIL} = 5mA

PAD DESCRIPTION

Pad No.	Pin No.	Name	Description
1		VSS	Ground
2		COIL1	External coil connections
3		COIL2	External coil connections
4		VDD	Supply voltage
5		TEST1	Test Pad
6		TEST2	Test Pad
7		TEST3	Test Pad
8		TEST4	Test Pad
9		TEST5	Test Pad

FUNCTIONAL DESCRIPTION

The circuit is built up out of several functional blocks, control logic, coil interface, the power-on reset, and the memory module (EEPROM), The chip activates automatically during power-up as a result of the built in power-on reset.

1. Coil Interface

Power is derived from a full wave rectifier bridge. Data modulation takes place by loading the coil inputs to the bridge with a modulating circuit. The coil interface includes on-chip high voltage protection. The system clock for the chip is derived by means of a clock extractor coupled to the rectifier circuit.The Clock extractor / prescaler is the time base generator for data reading. Data is read from the EEPROM to the coil interface where the rf signal is modulated by the data in either the Manchester coded or PSK mode. The chip is EEPROM (not part of data) programmed and locked for either Manchester coded or PSK mode application.

2. Memory Array

Data storage:

The data EEPROM is arranged in an 8X8 bit array composed of 8 columns of 8bit bytes. The 64 bits of data stored in the array can be configured in any way as agreed with the client, and is factory programmed and locked in that way. This gives OTP (One Time Programmable) security.

Dode control:

Additional mode control EEPROM is used to set the mode of data reading in either the Manchester or Phase Shift Keyed (PSK) mode. The mode is also OTP programmed at the factory according to client request.

3. Control logic

The control logic gets its clock from the clock extractor / prescaler and facilitates the reading of the data stored in the data EEPROM according to settings in the mode control EEPROM so as to differentiate between the Manchester or PSK mode of data reading.

TIMING SPECIFICATIONS

The COIL1 and COIL2 pads modulate the incoming rf signal with either Manchester encoded or PSK encoded data. The data will repeatedly be read out serially until the power is reduced sufficiently to activate the power on reset again. In the Manchester data mode there are 64 rf carrier cycles for each data bit. In the PSK mode there are 16 rf carrier cycles for each data bit.

Manchester Mode Timing vs PSK Mode Timing

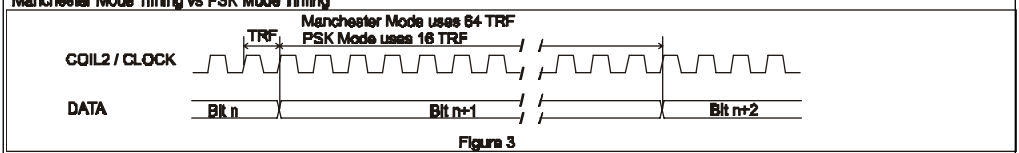
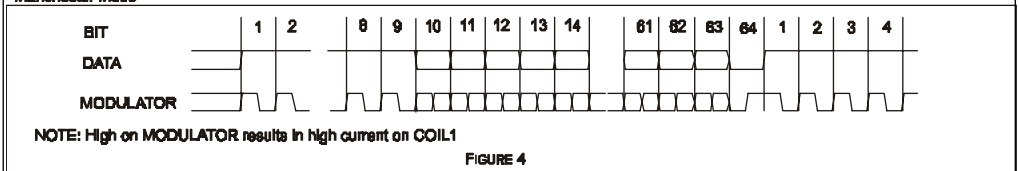


Figure 3

Manchester Mode



NOTE: High on MODULATOR results in high current on COIL1

FIGURE 4

PSK Mode

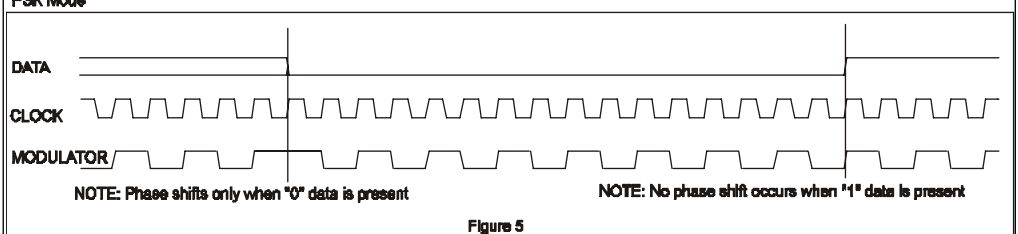


Figure 5

DR-01553

TYPICAL APPLICATION

The chip powers up via the COIL1 and COIL2 pads, deriving its energy from the rf carrier wave through the resonating tank circuit made up by the external inductor, LT, and external capacitor, CT. The data will automatically start modulating the rf signal as soon as the chip has powered up to the power-on reset level. The built in voltage protection and regulation insures protection against high voltage from the tank circuit.

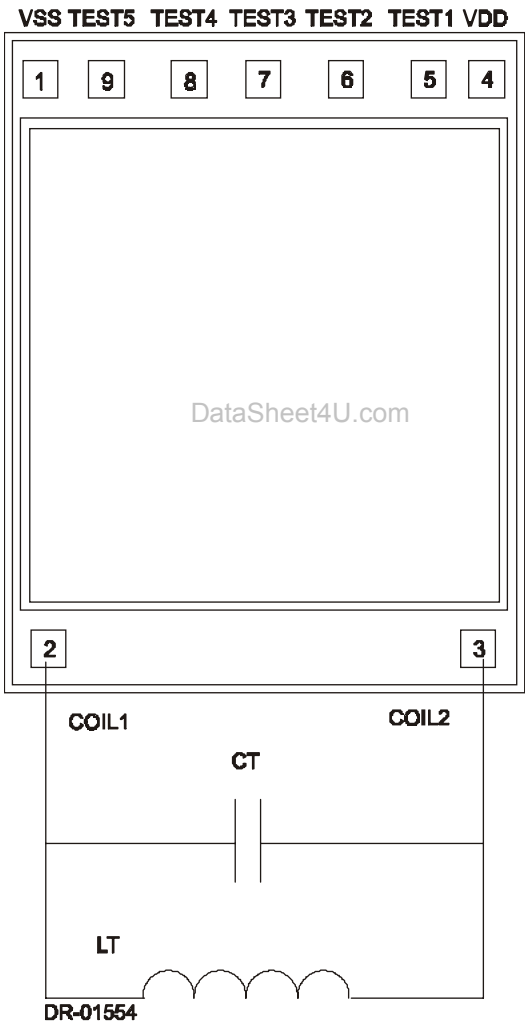


Figure 6

Note:

Any sales or technical questions may be posted to our e-mail adress below:
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http://www.sames.co.za

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